LUMENTUM

QSFP28 LR4 Optical Transceiver with 100GE for up to 10 km Reach, Single Protocol

TRQ5E20ENF-LF000

Lumentum 100GE QSFP+ 28 Gbps 4x (QSFP28) transceiver module TRQ5E20ENF enables a dense-port and high-throughput solution with its compact size and low power consumption. The TRQ5E20ENF modules can be used in various network applications, such as Internet Protocol switches and routers applications. The maximum transmission length of TRQ5E20ENF is 10km.

TRQ5E20ENF is a fully integrated 4 x 25 Gbps optical transceiver module that consists of 1310 nm wavelength LDs, Driver ICs, PIN photo-diodes, and clock and data recovery (CDR) ICs with 25 Gbps electrical interfaces.

Mechanical dimensions, connecters and footprint of TRQ5E20ENF conform to QSFP28 SFF specifications. The module size is 18.4 mm x 72 (122) mm x 8.5 mm and is hot pluggable in Z-direction by 38-pin connector.

Key Features

- 100 Gigabit Ethernet (100GE) 100GBASE-LR4 single protocol transceiver
- 103.125 Gbps single rate capability
- 25.78125 Gbps x 4 channel electrical interface (CAUI-4)
- Transmission length up to 10 km
- Optical light source: 4 channel x 1310 nm LD
- Optical receiver: 4 channel x PIN photo detector
- Operating case temperature: 0°C to 70°C
- Compact size: 18.4 mm x 72 (122) mm x 8.5 mm
- Hot Z-pluggable to 38-pin electrical connector
- Latching mechanism: pull tab
- 2-wire common management interface (SFF-8636)

Compliance

- IEEE Std. 802.3ba-2010 100GBASE-LR4
- IEEE Std 802.3bm-2015
- QSFP+ 28Gbps 4 pluggable transceiver specifications (SFF-8665 Rev 1.8 May 10, 2013)
- SFF-8636 Rev 2.5 April 18, 2015
- SFF-8679 Rev 1.7 August 12, 2014
- RoHS 6/6

1. Functional Description

1.1 Low Speed Pin Descriptions

In addition to the 2-wire serial interface the transceiver has the following low speed pins for control and status:

ModSelL
ResetL
LPMode
ModPrsL
IntL

1) ModSelL
The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL, is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModgelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

2) ResetL
The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

3) LPMode
The LPMode pin shall be pulled up to Vcc in the module. The pin is a hardware control used to put modules into a low power mode when high. By using the LPMode pin and a combination of the Power_override, Power_set and High_Power_Class_Enable software control bits (Address A0h, byte 93 bits 0,1,2), the host controls how much power a module can dissipate.

4) ModPrsL
ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModprsL is asserted "Low" when inserted and de-asserted "High" when the module is physically absent from the host connector.

5) IntL
IntL is an output pin. When IntL is "Low," it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. The IntL pin is de-asserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of "0" and the flag field is read (see SFF-8636).

1.2 High Speed Pin Electrical Specifications

1.2.1 Rx(n)(p/n)
Rx(n)(p/n) are module receiver data outputs. Rx(n)(p/n) are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC (SerDes). The AC coupling is inside the module and not required on the Host board. Output squelch for loss of optical input signal, hereafter Rx Squelch shall function as follows. In the event of the optical signal on any channel becoming equal to or less than the level required to assert LOS, then the receiver data output for that channel shall be squelched or disabled. In the squelched or disabled state output impedance levels are maintained while the differential voltage swing shall be less than 50 mVpp. In normal operation the default case has Rx Squelch active. Rx Squelch can be deactivated using Rx Squelch Disable through the 2-wire serial interface.

1.2.2 Tx(n)(p/n)

Tx(n)(p/n) are module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the module. The AC coupling is inside the module and not required on the Host board. Output squelch, hereafter Tx Squelch, for loss of input signal, hereafter Tx LOS, is supported. In the event of the differential, peak-to-peak electrical signal on any channel becomes less than 50 mVpp, then the transmitter optical output for that channel shall be squelched and the associated TxLOS flag set. Where squelched, the transmitter OMA shall be less than or equal to -26 dBm.

In module operation, the default case has Tx Squelch active. Tx Squelch can be deactivated using Tx Squelch Disable through the 2-wire serial interface. Tx Squelch Disable is an optional function.

1.3 Power Supply Pins

1.3.1 Power Classes and Maximum Power Consumption

QSFP28 modules are categorized into several power classes as listed in Table 1. The power class of TRQ5E2x is class 6.

Table 1 Maximum Power Classes

Power Class	Maximum power dissipation per module (W)
1	1.5
2	2.0
3	2.5
4	3.5
5	4.0
6	4.5
7	5.0

1.3.2 Module Power Supply Specification

In order to avoid exceeding the host system power capacity, upon hot-plug, power cycle or reset, all QSFP28 modules shall power up in power class 1, designated as “Low Power Mode”. TRQ5E2x will only reach fully functional operation after the host system enables “High Power Mode”. High power mode is defined as the maximum power class as advertised in page 00, byte 129 and will only be enabled by the host if the host can supply sufficient power to the module. The host system controls using the LPMode input pin and by writing to 3 control bits in byte 93. The management interface specification, SFF-8636 provides complete details but for explanation of power supply control.

1.4 Low Speed Control Pins

1.4.1 Low Speed Signaling

Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTL) operating at V_{cc}.

Table 2 Low Speed Pin Electrical Specifications

Parameter	Symbol	Minimum	Maximum	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL (max)=3.0mA
	VOH	V_{cc}-0.5	V_{cc}+0.3	V	
SCL and SDA	VIL	-0.3	V_{cc}*0.3	V	
	VIH	Vcc*0.7	V_{cc} + 0.5	V	
Capacitance for SCL and SDA I/O pin	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	3.0 k ohms pullup resistor, max
			200	pF	1.6 k ohms pullup resistor, max
LPMode, Reset and ModSeIL	VIL	-0.3	0.8	V	|Iin|<=125 uA for 0V<Vin, V_{cc}
	VIH	2	V_{cc}+0.3	V	
ModPrsL and IntL	VOL	0	0.4	V	iOL=2.0mA
	VOH	V_{cc}-0.5	V_{cc}+0.3	V	

1.4.2 2-Wire Management Interface

The QSFP28 Module supports alarm, control and monitor functions via a two-wire interface bus. Upon module initialization, these functions are available. QSFP28 two-wire electrical interface consists of 2 pins of SCL (2-wire serial interface clock) and SDA (2-wire serial interface data). The timing requirements on the two-wire interface are listed in Table 3 and Figure 1.

Table 3 2-Wire Interface Timing Requirements

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Clock frequency	fSCL	0	400	kHz	
Clock pulse width low	tLOW	1.3		µs	
Clock pulse width high	tHIGH	0.6		µs	
Time bus free before new transaction can start	tBUF	20		µs	Between STOP and START
START hold time	tHD,STA	0.6		µs	
START set-up time	tSU,STA	0.6		µs	
Data in hold time	tHD,DAT	0		µs	
Data in set-up time	tSU,DAT	0.1		µs	
Input rise time (400 kHz)	tR,400		300	ns	Note 1
Input fall time (400 kHz)	tF,400		300	ns	Note 2
STOP set-Up time	tSU,STO	0.6		µs	
Serial interface clock holdoff "clock stretching"	T_clock_hold		500	µs	Maximum time the slave (QSFP28) may hold the SCL line low before continuing read or write operation
Complete single or sequential write	tWR		40	ms	Complete (up to) 4 Byte Write
Endurance (write cycles)		50 k		Cycles	70°C

Note:
1. From (VIL,MAX – 0.15) to (VIH,MIN + 0.15)
2. From (VIH,MIN + 0.15) to (VIL,MAX - 0.15)

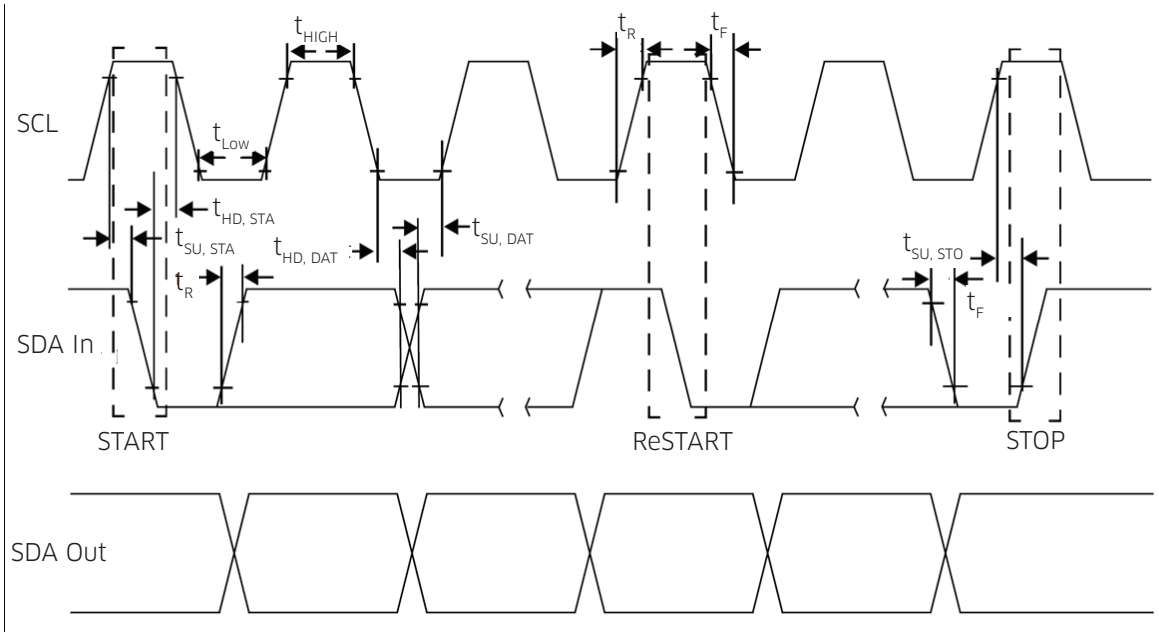


Figure 1 2-Wire interface timing diagram

PERFORMANCE SPECIFICATIONS

2 Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device.

Table 4 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit	Remarks
Supply voltage	V_{cc}	0	+3.6	V	+3.3 V
Storage temperature		-40	85	°C	
Optical receiver input			+5.5	dBm	Average

3 Operating Environments

Electrical and optical characteristics below are defined under this operating environment, unless otherwise specified.

Table 5 Operating Environment

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Remarks
Supply voltage	V_{cc}	3.135	3.3	3.465	V	
Supply voltage noise tolerance	PSNR			66	mV	10 Hz – 10 MHz
Case temperature	TC	0	25	70	°C	

4 Electrical Characteristics

Table 6 Electrical Characteristics

No	Parameter	Minimum	Typical	Maximum	Unit	Remarks
Transmitter (each lane)						
1	Differential pk-pk input voltage tolerance (min)	900			mV	at TP1a
2	Differential termination mismatch			10	%	at TP1
3	Single-ended input voltage tolerance range	-0.4 to 3.3			V	at TP1a
4	DC common mode voltage	-350		2850	mV	at TP1
Receiver (each lane, at TP4)						
1	AC Common-mode output voltage (RMS)			17.5	mV	
2	Differential output voltage			900	mV	
3	Eye width	0.57			UI	
4	Eye height, differential	228			mV	
5	Vertical eye closure			5.5	dB	
6	Differential termination mismatch			10	%	
7	Transition time (20% to 80%)	12			ps	
8	DC common mode voltage	-350		2850	mV	

Note:
1. Electrical Rx output is squelched for loss of optical input signal.

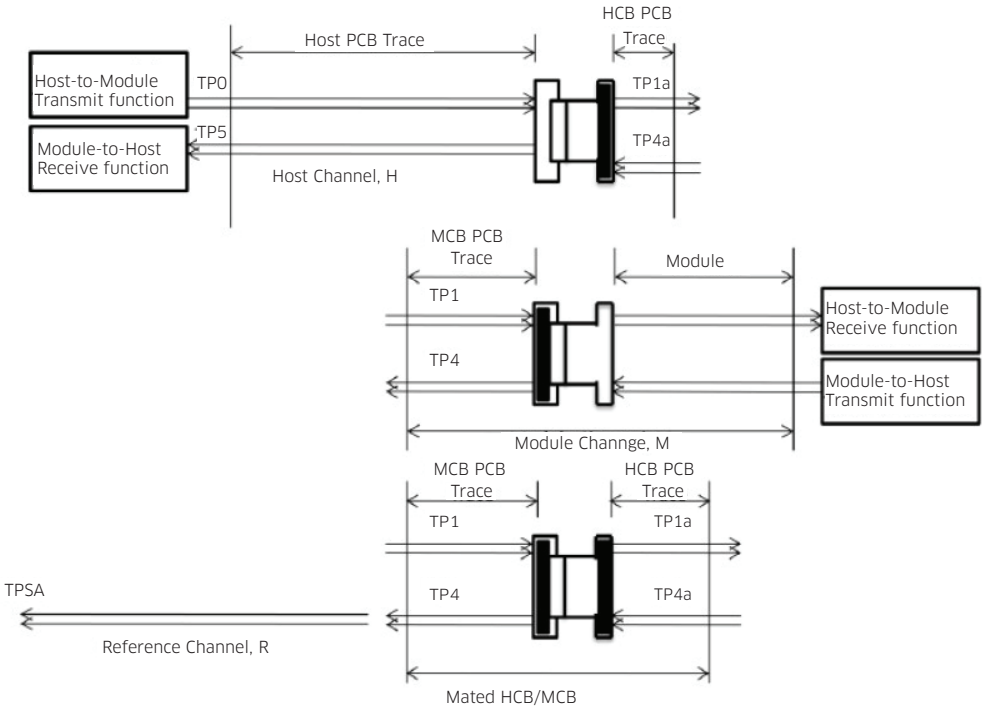


Figure 2 Reference points

5 Optical Characteristics

Table 7 Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Remarks
Channel data rate	fDC	25.78125			Gbps	IEEE 802.3ba
Aggregate data rate	fD	103.125			Gbps	
Signal speed variation from nominal	ΔfD	-100		+100	ppm	
Transmitter center wavelength						
Lane 0	λ_{CT0}	1294.53		1296.59	nm	
Lane 1	λ_{CT1}	1299.02		1301.09		
Lane 2	λ_{CT2}	1303.54		1305.63		
Lane 3	λ_{CT3}	1308.09		1310.19		
Optical output power in OMA	OMA	-1.3		+4.5	dBm	Note 2
Average optical output power of off transmitter	P_{off}			-30	dBm	
Optical waveform		Figure 3				IEEE 802.3ba
Extinction ratio	ER	4			dB	
Receiver sensitivity in OMA	P_{minOMA}	-8.6		+4.5	dBm	
Stressed receiver sensitivity in OMA	$P_{minSOMA}$			-6.8	dBm	Note 3
Receive power, each lane in OMA				+4.5	dBm	

Note:
1. Data rate; NRZ, Mark ratio 50%, PRBS=2^{31}-1, 1x10^{-12} BER unless otherwise specified.
2. OMA=$10\log_{10}[2P\{(A-1)/(A+1)\}]$, A = $10^{(ER/10)}$, P = $10^{(Pf/10)}$
3. Stressed receiver sensitivity measurement method is under study.

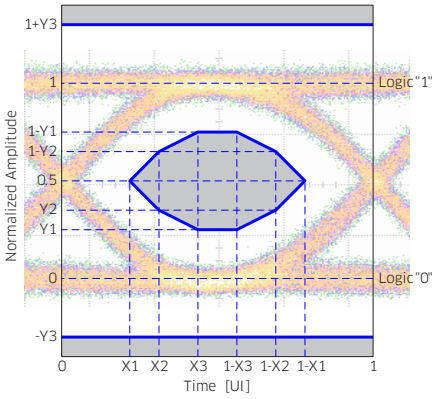


Figure 3 Mask of optical output eye diagram

X1	X2	X3	Y1	Y2	Y3	Maximum hit ratio[1]
0.25	0.4	0.45	0.25	0.28	0.4	5×10^{-5}

Note:
1. The acceptable ratio of samples inside to outside the hatched area (the "hit ratio") must be met.

6 Pin Assignment

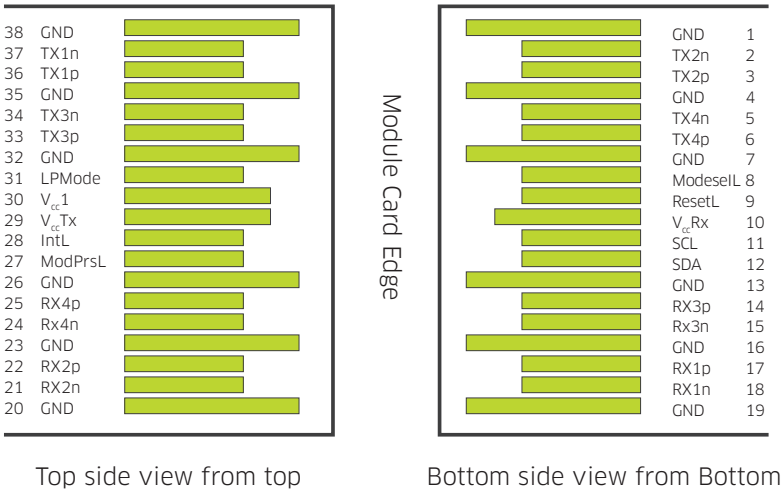


Figure 4 Pin configuration

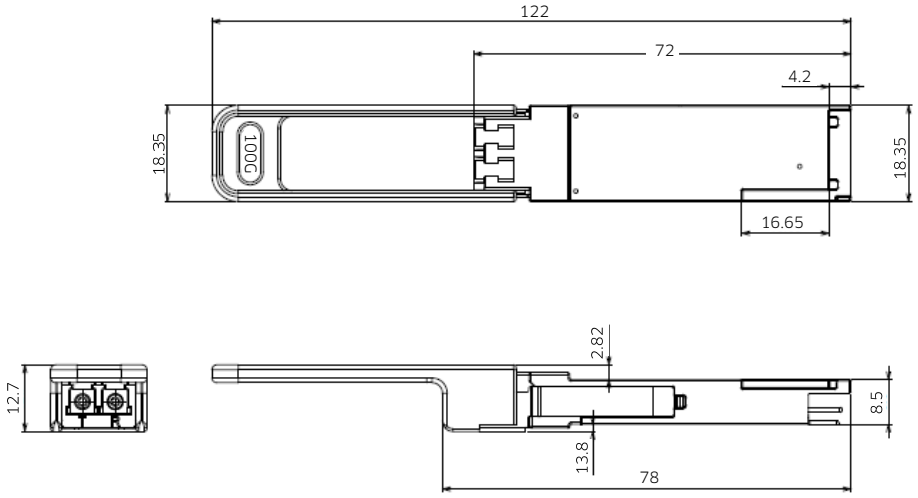
Table 8 Pin Descriptions

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter inverted data input	3	
3	CML-I	Tx2p	Transmitter non-inverted data input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter inverted data input	3	
6	CML-I	Tx4p	Transmitter non-inverted data input	3	
7		GND	Ground	1	1
8	LVTTL-I	Modse1L	Module select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		V_{cc} Rx	+3.3V power supply receiver	2	2
11	LVCMO S-I/O	SCL	2-wire serial interface clock	3	
12	LVCMO S-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver non-inverted data output	3	
15	CML-O	Rx3n	Receiver inverted data output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver non-inverted data output	3	
18	CML-O	Rx1n	Receiver inverted data output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver inverted data output	3	
22	CML-O	Rx2p	Receiver non-inverted data outout	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver inverted data output	3	
25	CML-O	Rx4p	Receiver non-inverted data output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		V_{cc} Tx	+3.3V power supply transmitter	2	2
30		V_{cc}1	+3.3V power supply	2	2
31	LVTTL-I	LPMode	Low power mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter non-inverted data input	3	
34	CML-I	Tx3n	Transmitter inverted data input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter non-inverted data input	3	
37	CML-I	Tx1n	Transmitter inverted data input	3	
38		GND	Ground	1	1

Note:
1. GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. V_{cc} Rx, V_{cc}1 and V_{cc} Tx shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 5-6. V_{cc} Rx V_{cc}1 and V_{cc} Tx may be internally connected within the module in any combination. The connector pins are each rated for a maximum current of 100 mA.

7 Mechanical Dimensions

Unit: mm



Pull tab color: Blue

Figure 5 Mechanical dimensions

8 Handling Precautions

CAUTION: Take proper electrostatic-discharge (ESD) precautions while handling these devices. These devices are sensitive to ESD. The module meets ESD requirements given in EN6100-4-2, criterion B test specification when installed in a properly grounded case and chassis. The module high speed signal contacts shall withstand 1000 V electrostatic discharge based on human Body model per JEDEC JESD22-A114-B.

9 EMI Compliance

This product meets electromagnetic interference (EMI) specifications of following standards.

1 FCC Part 15, Subpart B (Class B)
2 EN5502 (Class B)

10 Laser Safety

This product is complied with IEC 60825-1 as Class 1 and with FDA 21 CFR as Class I laser product.
Because of size constraints, laser safety labeling is not affixed to the module but is attached to the outside of the shipping box.

Ordering Information:
For more information on this or other products and their availability, please contact your local Lumentum account manager or Lumentum directly at customer.service@lumentum.com.

Description	Part number
QSFP28 optical transceiver, 100GE, 10 km reach, LR4, commercial temperature range, pull tab	TRQ5E20ENF-LF000

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