10G SFP+ Transceiver

MTRS-2E30-01

Features

- 10Gb/s serial optical interface
- 1310nm DFB transmitter, PIN photo-detector
- Transmission distance up to 10Km with SMF
- LC duplex conector
- Integrated clock and data recovery (CDR) function
- Operating case temperature:
  0°C~70°C

Applications

- SONET(OC-192)/SDH(STM64)
- 10GBASE-LR (10.3125Gbps)
- 10GBASE-LW (9.953Gbps)

Compliance

- Compliant with IEEE 802.3ae-2002 10G Base-LR
- Compliant with SFF-8431 & SFF-8083 & SFF-8432 & SFF 8472
- Compliant with RoHS

Description

The MTRS-2E30-01 is a very compact 10Gb/s optical transceiver module for serial optical communication applications at 10Gb/s. The MTRS-2E30-01 series converts a 10Gb/s serial electrical data stream to 10Gb/s optical output signal and a 10Gb/s optical input signal to 10Gb/s serial electrical data streams. The high speed 10Gb/s electrical interface is fully compliant with XFI specification (built in CDR on both TX and RX) and allows FR4 host PCB trace up to 200mm. The MTRS-2E30-01 is designed for use in a variety of 10Gb/s equipment SDH/SONET (9.95Gb/s), Ethernet LAN (10.3Gb/s) and FC (10.5Gb/s). The customer can adjust interface' electrical level to select 8.5G~11.3G rate section. The high performance 1310nm DFB transmitter coupled with a high sensitivity PIN receiver provide superior performance for applications up to 10km with SMF. The fully compliant SFP form factor provides high density applications, hot plug ability easy optical port upgrades and low EMI emission.

The SFP+ LR w/CDR module electrical interface is compliant to XFI electrical specifications. The transmitter input and receiver output impedance is 100Ohms differential. Data lines are internally AC coupled. The module provides differential termination and reduce differential to common mode conversion for quality signal termination and low EMI. XFI typically operates over 200 mm of improved FR4 material or up to about 150mmof standard FR4 with one connector.

Specification

Table1-Absolute Maximum Ratings

Parameter	Symbol	Min.	Typical	Max.	Unit
Storage Temperature	Ts	-40	-	+85	℃
Operating Case Temperature	Tc	0	-	+70	℃
Supply Voltage	Vcc	0	-	3.6	V
Relative Humidity	RH	5	-	+95	%
Rx Input Average Power	Pmax	-	-	+3	dBm

Table2-Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	T_C	0	25	+70	℃
Power Supply Voltage	V_{CC3}	3.135	3.3	3.465	V
Power Supply Current	I_{CC3}	-	-	430	mA
Power Consumption		-	-	1500	mW

Table3-Transmitter Operating Characteristic-Optical, Electrical

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Operating Data Rate	DR	8.5	9.953	11.3	Gb/s	1
Output Center Wavelength	λ c	1290	1310	1330	nm	
Spectral Width	⊿λ	-	-	1	nm	
Side Mode Suppression Ratio	SMSR	30	-	-	dB	
Average Output Power	Po	-6	-	-1	dBm	2
Disabled Power	Poff	-	-	-30	dBm	2
Extinction Ratio	ER	6	-	-	dB	2
Minimum OMA-TDP (10G Ethernet)	OMAtdp	-5.2	-	-	dBm	3
Eye Mask (@SONET/SDH)	GR-253-CORE/ITU-T G.691					2
Eye Mask (@10G Ethernet)	IEEE802.3ae					3
Generation Jitter 1 (20kHz - 80MHz)	-	-	-	0.3	UIp-p	2,4
Generation Jitter 2 (4MHz - 80MHz)	-	-	-	0.1	UIp-p	2,4
Relative Intensity Noise	RIN	-	-	-128	dB/Hz	
Chromatic Dispersion (SONET/SDH)	CD	-	-	6.6	ps/nm	
Operating Distance	-	-	-	10	km	

Attenuation (SONET/SDH)	-	0	-	4	dB	
Channel Insertion Loss (10G Ethernet)	-	0	-	6	dB	
Maximum DGD (SONET/SDH)	DGD	-	-	30	ps	
Single Ended Output Voltage Tolerance	-	-0.3	-	4	V	
Common mode voltage tolerance	-	15	-	-	mV	
Tx Input Diff Voltage	VI	120	-	820	mV	
Tx Fault	Vol	-0.3	-	0.4	V	At 0.7mA
Data Dependent Input Jitter	DDJ	-	-	0.1	UI	
Data Input Total Jitter	TJ	-	-	0.28	UI	

Table4-Receiver Operating Characteristic-Optical, Electrical

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
Operating Data Rate	-	8.5	9.953	11.3	Gb/s	1
Input Center Wavelength	Irc	1260		1620	nm	
Overload	Rovl	0.5	-	-	dBm	
Minimum Sensitivity	Rsen	-	-	-14.4	dBm	2
Sensitivity in OMA	OMA0	-	-	-12.6	dBm	3
Stressed Sensitivity in OMA	OMAst	-	-	-10.3	dBm	3
RX_LOS Assert	RLOSa	-30	-	-	dBm	4
RX_LOS Deassert	RLOSd	-	-	-16	dBm	
RX_LOS Hysteresis	RLOSh	0.5	-	5	dB	
Optical Path Penalty	DP	-	-	1	dB	1
Optical Return Loss	ORL		-	-14	dB	
Jitter Tolerance	GR-253-CORE/ITU-T G.783					
Single Ended Output Voltage Tolerance	-	-0.3	-	4	V	
Rx Output Diff Voltage	Vo	340	-	850	mV	
Data output rise/fall time		30			ps	20%~80%
Total Jitter	TJ	-	-	0.7	UI	
Deterministic Jitter	DJ	-	-	0.42	UI	

Notes:

[1]Data rate tolerance 10GBASE-LR/LW: typ.+/-100ppm

[2]Measured at 9.953Gbps,Non-framed PRBS2^31-1,NRZ

[3]Measured by using SFP+ evaluation board.

[4]When LOS assert, the RX shall not mask its data output. LOS output from LA, and LA connect to TIA using AC Coupling, so asserting LOS depend on receiving data.

Table5-Control and Status I/O Timing Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Note
TX Disable Assert Time	t_off		-	10	μs	1
TX Disable Negate Time	t_on		-	1	ms	2
Time to initialize including reset of TX_Fault	t_init		-	300	ms	3
TX Fault Assert Time	t_fault		-	100	μs	4
TX Disable to Reset	t_reset	10	-		μs	5
LOS Assert Time	t_loss_on		-	100	μs	6
LOS Deassert Time	t_loss_off		-	100	μs	7
Rate-Select Change Time	t_ratesel		-	10	μs	8
Serial ID Clock Rate	f_serial_ clock		-	100	kHz	

Notes:

[1] Time from rising edge of TX Disable to when the optical output falls below 10% of nominal

[2] Time from falling edge of TX Disable to when the modulated optical output rises above 90% of nominal

[3] From power on or negation of TX Fault using TX Disable

[4] Time from fault to TX fault on

[5] Time TX Disable must be held high to reset TX_fault

[6] Time from LOS state to RX LOS assert

[7] Time from non-LOS state to RX LOS deassert.

[8] Time from rising or falling edge of Rate Select input until receiver bandwidth is in conformance with appropriate specification

Digital Diagnostic Function

The following digital diagnostic characteristics are defined over the Recommended Operating Environment unless otherwise specified. It is compliant to SFF-8472 Rev11.1 with internal calibration mode. For external calibration mode please contact our sales stuff.

Table6: Digital diagnostic specification table

Parameter	Symbol	Min.	Max	Unit	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	degC	
Laser power monitor absolute error	DMI_TX	-2	2	dB	
RX power monitor absolute error	DMI_RX	-2	2	dB	
Supply voltage monitor absolute error	DMI_VCC	-3%	-3%	V	
Bias current monitor	DMI_Ibias	-10%	10%	mA	

EEPROM Information

Table7: EEPROM Serial ID Memory Contents (A0h)

Data Address	Size (Bytes)	Name of Field	Contents(Hex)	Description
BASE ID FIELDS				
0	1	Identifier	03	SFP

1	1	Ext. Identifier	04	SFP function is defined by serial ID only
2	1	Connector	07	LC Connector
3-10	8	Transceiver	20 30 00 00 00 00 00 00	-
11	1	Encoding	05	-
12	1	BR, Nominal	67	-
13	1	Reserved	06	Rx & Tx Rate_select
14	1	Length (9μm) km	0A	10km
15	1	Length (9μm) 100m	64	100(100m)
16	1	Length (50μm) 10m	00	-
17	1	Length(62.5μm)10m	00	-
18	1	Length (Copper)	00	-
19	1	Reserved	00	-
20-35	16	Vendor name	48 47 20 47 45 4E 55 49 4E 45 20 20 20 20 20 20	“HG GENUINE” (ASCII)
36	1	Reserved	00	-
37-39	3	Vendor OUI	00 00 00	-
40-55	16	Vendor PN	4D 54 52 53 2D 32 45 33 30 2D 30 31 20 20 20 20	“MTRS-2E30-01” (ASCII)
56-59	4	Vendor rev	00 00 00 00	-
60-61	2	Wavelength	05 1E	1310nm Laser wavelength
62	1	Reserved	00	-
63	1	CC_BASE	36	-
EXTENDED ID FIELDS				
64-65	2	Options	00 1A	TX_DISABLE, TX_FAULT and Loss of Signal implemented.
66	1	BR,max	00	-
67	1	BR,min	00	-
68-83	16	Vendor SN	30 30 34 39 34 39 30 35 20 20 20 20 20 20 20 20	Serial Number of transceiver (ASCII). For example “00494905”.
84-91	8	Date code	30 32 31 30 30 35 20 20	Manufactory date code. For example “021005”.
92	1	Diagnostic Monitoring Type	68	Internally Calibrated
93	1	Enhanced Options	F0	Optional Alarm/Warning flags implemented for all monitored quantities, Optional Soft TX_FAULT monitoring implemented, Optional Soft RX_LOS monitoring implemented.
94	1	SFF_8472 Compliance	04	Includes functionality described in Rev10.4 SFF-8472.
95	1	CC_EXT	Check Sum (Variable)	Check sum for Extended ID Field.
VENDOR SPECIFIC ID FIELDS				
96-127	32	Vendor Specific	Read only	Depends on customer information

128-255	128	Reserved	Read only	Filled by zero

Alarm/warning threshold

Address	Field Size (Byte)	Bits	Name of Field	Description
00~01	2	ALL	Temp High Alarm Thresholds	MSB at low address,80℃
02~03	2	ALL	Temp Low Alarm Thresholds	MSB at low address,-10℃
04~05	2	ALL	Temp High Warning Thresholds	MSB at low address,70℃
06~07	2	ALL	Temp Low Warning Thresholds	MSB at low address,0℃
08~09	2	ALL	Voltage High Alarm Thresholds	MSB at low address,3.63V
10~11	2	ALL	Voltage Low Alarm Thresholds	MSB at low address,2.97V
12~13	2	ALL	Voltage High Warning Thresholds	MSB at low address,3.465V
14~15	2	ALL	Voltage Low Warning Thresholds	MSB at low address,3.135V
16~17	2	ALL	Bias High Alarm Thresholds	MSB at low address,100mA
18~19	2	ALL	Bias Low Alarm Thresholds	MSB at low address,2mA
20~21	2	ALL	Bias High Warning Thresholds	MSB at low address,90mA
22~23	2	ALL	Bias Low Warning Thresholds	MSB at low address,3mA
24~25	2	ALL	TX Power High Alarm Thresholds	MSB at low address,1.0dBm
26~27	2	ALL	TX Power Low Alarm Thresholds	MSB at low address,-8dBm
28~29	2	ALL	TX Power High Warning Thresholds	MSB at low address, -1dBm
30~31	2	ALL	TX Power Low Warning Thresholds	MSB at low address, -6dBm
32~33	2	ALL	RX Power High Alarm Thresholds	MSB at low address,2.5dBm
34~35	2	ALL	RX Power Low Alarm Thresholds	MSB at low address,-16.4dBm
36~37	2	ALL	RX Power High Warning Thresholds	MSB at low address,0.5 dBm
38~39	2	ALL	RX Power Low Warning Thresholds	MSB at low address, -14.4dBm
40~55	16	ALL	Reserved	MSB at low address
56~59	4	ALL	Rx_PWR(4)	Single precision floating point calibration data - Rx optical power. Bit7 of byte 56 is MSB. Bit 0 of byte 59 is LSB. For “internally calibrated” devices, Rx_PWR(4) should be set to zero , and useless.
60~63	4	ALL	Rx_PWR(3)	Single precision floating point calibration data - Rx optical power.Bit 7 of byte 60 is MSB. Bit 0 of byte 63 is LSB. For “internally calibrated” devices,Rx_PWR(3) should be set to zero , and useless.
64~67	4	ALL	Rx_PWR(2)	Single precision floating point calibration data, Rx optical power.Bit 7 of byte 64 is MSB, bit 0 of byte 67 is LSB. For “internally calibrated” devices, Rx_PWR(2) should be set to zero, and useless .
68~71	4	ALL	Rx_PWR(1)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 68 is MSB, bit 0 of byte 71 is LSB. For “internally calibrated” devices, Rx_PWR(1) should be set to 1 , and useless.
72~75	4	ALL	Rx_PWR(0)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 72 is MSB, bit 0 of byte 75 is LSB. For “internally calibrated” devices,Rx_PWR(0) should be set to zero , and useless.

Address	Field Size (Byte)	Bits	Name of Field	Description
76~77	2	ALL	Tx_I(Slope)	Fixed decimal (unsigned) calibration data, laser bias current. Bit 7 of byte 76 is MSB, bit 0 of byte 77 is LSB. For “internally calibrated” devices, Tx_I(Slope) should be set to 1, and useless.
78~79	2	ALL	Tx_I(Offset)	Fixed decimal (signed two’s complement) calibration data, laser bias current. Bit 7 of byte 78 is MSB, bit 0 of byte 79 is LSB. For “internally calibrated” devices,Tx_I(Offset)should be set to zero , and useless.
80~81	2	ALL	Tx_PWR(Slope)	Fixed decimal (unsigned) calibration data, transmitter coupled output power. Bit 7 of byte 80 is MSB, bit 0 of byte 81 is LSB.For “internally calibrated” devices, Tx_PWR(Slope) should be set to 1 , and useless.
82~83	2	ALL	Tx_PWR(Offset)	Fixed decimal (signed two’s complement) calibration data, transmitter coupled output power. Bit 7 of byte 82 is MSB, bit 0 of byte 83 is LSB. For “internally calibrated” devices,Tx_PWR(Offset) should be set to zero , and useless.
84~85	2	ALL	T (Slope)	Fixed decimal (unsigned) calibration data, internal module temperature. Bit 7 of byte 84 is MSB, bit 0 of byte 85 is LSB.For “internally calibrated” devices, T(Slope) should be set to 1 , and useless.
86~87	2	ALL	T (Offset)	Fixed decimal (signed two’s complement) calibration data, internal module temperature. Bit 7 of byte 86 is MSB, bit 0 of byte 87 is LSB. For “internally calibrated” devices, T(Offset) should be set to zero , and useless.
88~89	2	ALL	V (Slope)	Fixed decimal (unsigned) calibration data, internal module supply voltage. Bit 7 of byte 88 is MSB, bit 0 of byte 89 is LSB. For “internally calibrated” devices, V(Slope)should be set to 1 , and useless.
90~91	2	ALL	V (Offset)	Fixed decimal (signed two’s complement) calibration data, internal module supply voltage. Bit 7 of byte 90 is MSB. Bit 0 of byte 91 is LSB. For “internally calibrated” devices, V(Offset) should be set to zero , and useless.
92~94	3	ALL	Reserved	Reserved
95	1	ALL	Checksum	Byte 95 contains the low order 8 bits of the sum of bytes 0 – 94.
96	1	ALL	Temperature MSB	Internally measured module temperature.
97	1	ALL	Temperature LSB	
98	1	ALL	Vcc MSB	Internally measured supply voltage in transceiver.
99	1	ALL	Vcc LSB	
100	1	ALL	TX Bias MSB	Internally measured TX Bias Current.
101	1	ALL	TX Bias LSB	

Address	Field Size (Byte)	Bits	Name of Field	Description
102	1	ALL	TX Power MSB	Measured TX output power.
103	1	ALL	TX Power LSB	
104	1	ALL	RX Power MSB	Measured RX input power.
105	1	ALL	RX Power LSB	
106~109	4	ALL	Reserved	Reserved
110	1	7	TX Disable State	Digital state of the TX Disable Input Pin. Updated within 100ms of change on pin.
		6	Soft TX Disable	Read/write bit that allows software disable of laser. Writing '1' disables laser. This bit is "OR"d with the hard TX_DISABLE pin value. Note, per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is zero/low.
		5	RS(1) Stated	Digital state of SFP input pin AS(1) per SFF-8079 or RS(1) per SFF-8431. Updated within 100ms of change on pin. See A2h Byte 118, Bit 3 for Soft RS(1) Select control information.
		4	Rate Select State	Digital state of the SFP Rate_Select Input Pin. Updated within 100ms of change on pin. Note: This pin is also known as AS(0) in SFF-8079 and RS(0) in SFF-8431.
		3	Soft Rate Select	Read/write bit that allows software rate select control. Writing '1' selects full bandwidth operation. This bit is "OR'd with the hard Rate_Select, AS(0) or RS(0) pin value. See Table 3.11 for timing requirements. Default at power up is logic zero/low. If Soft Rate Select is not implemented, the transceiver ignores the value of this bit. Note: Specific transceiver behaviors of this bit are identified in Table 3.6a and referenced documents. See Table 3.18a, byte 118, bit 3 for Soft RS(1) Select.
		2	TX Fault	Digital state of the TX Fault Output Pin. Updated within 100ms of change on pin.
		1	LOS	Digital state of the RX_LOS Output Pin. Updated within 100ms of change on pin.
		0	Data_Ready_Bar	Reserved
111	1	ALL	Reserved	Reserved
112	1	7	Temp High Alarm	Set when internal temperature exceeds high alarm level.
		6	Temp Low Alarm	Set when internal temperature is below low alarm level.
		5	Vcc High Alarm	Set when internal supply voltage exceeds high alarm level.
		4	Vcc Low Alarm	Set when internal supply voltage is below low alarm level.
		3	TX Bias High Alarm	Set when TX Bias current exceeds high alarm level.
		2	TX Bias Low Alarm	Set when TX Bias current is below low alarm level.

Address	Field Size (Byte)	Bits	Name of Field	Description
		1	TX Power High Alarm	Set when TX output power exceeds high alarm level.
		0	TX Power Low Alarm	Set when TX output power is below low alarm level.
113	1	7	RX Power High Alarm	Set when Received Power exceeds high alarm level.
		6	RX Power Low Alarm	Set when Received Power is below low alarm level.
		5	Reserved	Reserved
		4	Reserved	Reserved
		3	Reserved	Reserved
		2	Reserved	Reserved
		1	Reserved	Reserved
		0	Reserved	Reserved
114	1	ALL	Reserved	Reserved
115	1	ALL	Reserved	Reserved
116	1	7	Temp High Warning	Set when internal temperature exceeds high warning level.
		6	Temp Low Warning	Set when internal temperature is below low warning level.
		5	Vcc High Warning	Set when internal supply voltage exceeds high warning level.
		4	Vcc Low Warning	Set when internal supply voltage is below low warning level.
		3	TX Bias High Warning	Set when TX Bias current exceeds high warning level.
		2	TX Bias Low Warning	Set when TX Bias current is below low warning level.
		1	TX Power High Warning	Set when TX output power exceeds high warning level.
		0	TX Power Low Warning	Set when TX output power is below low warning level.
117	1	7	RX Power High Warning	Set when Received Power exceeds high warning level.
		6	RX Power Low Warning	Set when Received Power is below low warning level.
		5	Reserved	Reserved
		4	Reserved	Reserved
		3	Reserved	Reserved
		2	Reserved	Reserved
		1	Reserved	Reserved
		0	Reserved	Reserved
118	1	7	Reserved	Reserved
		6	Reserved	Reserved
		5	Reserved	Reserved
		4	Reserved	Reserved
		3	Soft RS(1) Select	Read/write bit that allows software Tx rate control. Writing ‘1’ selects full speed Tx operation. This bit is “OR’d with the hard RS(1) pin value. Default at power up is logic zero/low. If Soft RS(1) is not implemented, the transceiver ignores the value of this bit.
		2	Reserved	Reserved

Address	Field Size (Byte)	Bits	Name of Field	Description
		1	Reserved	Reserved
		0	Reserved	Reserved
119	1	ALL	Reserved	Reserved
120-127	8	ALL	Vendor Specific	Vendor Specific
128-247	120	ALL	User EEPROM	User writable EEPROM
248-255	8	ALL	Vendor Specific	Vendor Specific

Pin-out Definition

The SFP+ modules are hot-pluggable. Hot pluggable refers to plugging in or unplugging a module while the host board is powered. The SFP+ host connector is a 0.8 mm pitch 20 position right angle improved connector specified by SFF-8083, or stacked connector with equivalent with equivalent electrical performance. Host PCB contact assignment is shown in Figure 1 and contact definitions are given in Table7. SFP+ module contacts mates with the host in the order of ground, power, followed by signal as illustrated by Figure 2 and the contact sequence order listed in Table7.

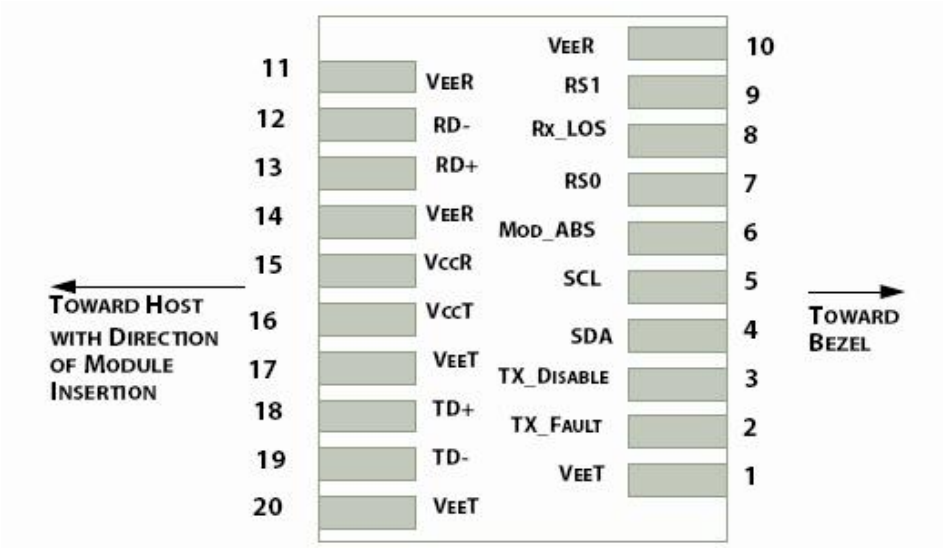

Figure1: Module Interface to Host

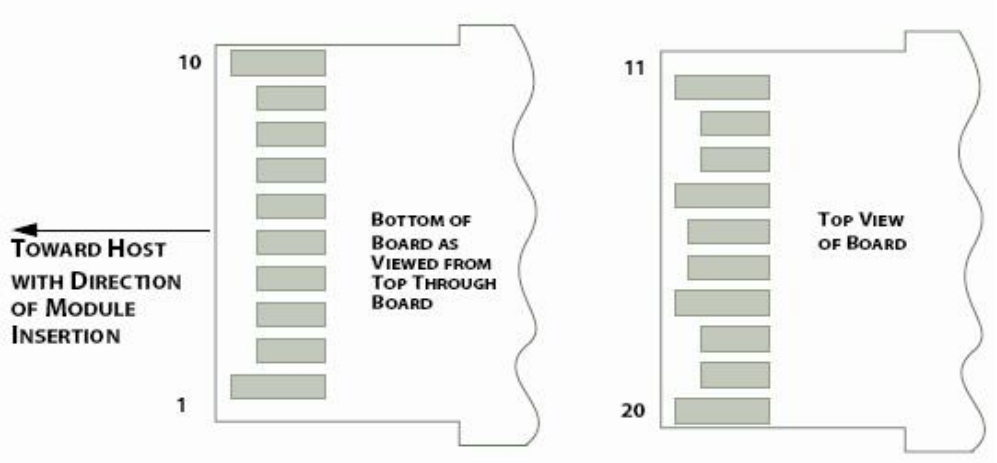

Figure2: Module Contact Assignment

Pin Assignment

Table7——SFP+ Module PIN Definition

PIN	Logic	Symbol	Name / Description	Note
1		VeeT	Module Transmitter Ground	1
2	LVTTL-O	TX_Fault	Module Transmitter Fault	
3	LVTTL-I	TX_Dis	Transmitter Disable; Turns off transmitter laser output	
4	LVTTL-I/O	SDA	2-Wire Serial Interface Data Line	2
5	LVTTL-I	SCL	2-Wire Serial Interface Clock	2
6		MOD_DEF0	Module Definition, Grounded in the module	
7	LVTTL-I	RS0	Receiver Rate Select	
8	LVTTL-O	RX_LOS	Receiver Loss of Signal Indication Active High	
9	LVTTL-I	RS1	Transmitter Rate Select	
10		VeeR	Module Receiver Ground	1
11		VeeR	Module Receiver Ground	1
12	CML-O	RD-	Receiver Inverted Data Output	
13	CML-O	RD+	Receiver Data Output	
14		VeeR	Module Receiver Ground	1
15		VccR	Module Receiver 3.3 V Supply	
16		VccT	Module Receiver 3.3 V Supply	
17		VeeT	Module Transmitter Ground	1
18	CML-I	TD+	Transmitter Non-Inverted Data Input	
19	CML-I	TD-	Transmitter Inverted Data Input	
20		VeeT	Module Transmitter Ground	1

Notes:

[1]Module ground pins GND are isolated from the module case.

[2]Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.

[3]When RS0=0 RS1=0, 8G FC for both TX and RX

When RS0=0 RS1=1, Bypass CDR in both TX and RX

When RS0=1 RS1=0, Bypass CDR in both TX and RX

When RS0=1 RS1=1, 9.95Gbps and 11.3Gbps for both TX and RX.

Block Diagram of Transceiver

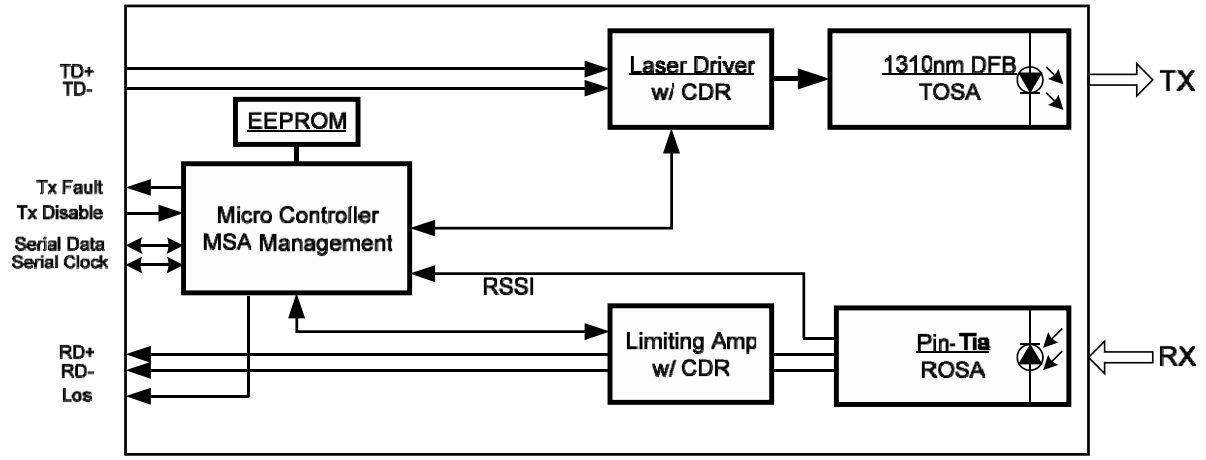

Figure3

Transmitter Section

The transmitter converts 10Gbit/s serial PECL or CML electrical data into serial optical data compliant with the 10GBASE-LR standard. An open collector compatible Transmit Disable (Tx_Dis) is provided. A logic "1," or no connection on this pin will disable the laser from transmitting. A logic "0" on this pin provides normal operation. The transmitter has an internal automatic power control loop (APC) to ensure constant optical power output across supply voltage and temperature variations. An open collector compatible Transmit Fault (Tx_Fault) is provided. TX_Fault is a module output contact that when high, indicates that the module transmitter has detected a fault condition related to laser operation or safety. The TX_Fault output contact is an open drain/collector and shall be pulled up to the Vcc_Host in the host with a resistor in the range 4.7-10 kΩ. TX_Disable is a module input contact. When TX_Disable is asserted high or left open, the SFP+ module transmitter output shall be turned off. This contact shall be pulled up to VccT with a 4.7 kΩ to 10 kΩ resistor

Receiver Section

The receiver converts 10Gbit/s serial optical data into serial PECL/CML electrical data. An open collector compatible Loss of Signal is provided. Rx_LOS when high indicates an optical signal level below that specified in the relevant standard. The Rx_LOS contact is an open drain/collector output and shall be pulled up to Vcc_Host in the host with a resistor in the range 4.7-10 kΩ, or with an active termination. Power supply filtering is recommended for both the transmitter and receiver. The Rx_LOS signal is intended as a preliminary indication to the system in which the SFP+ is installed that the received signal strength is below the specified range. Such an indication typically points to non-installed cables, broken cables, or a disabled, failing or a powered off transmitter at the far end of the cable.

Recommended Interface Circuit

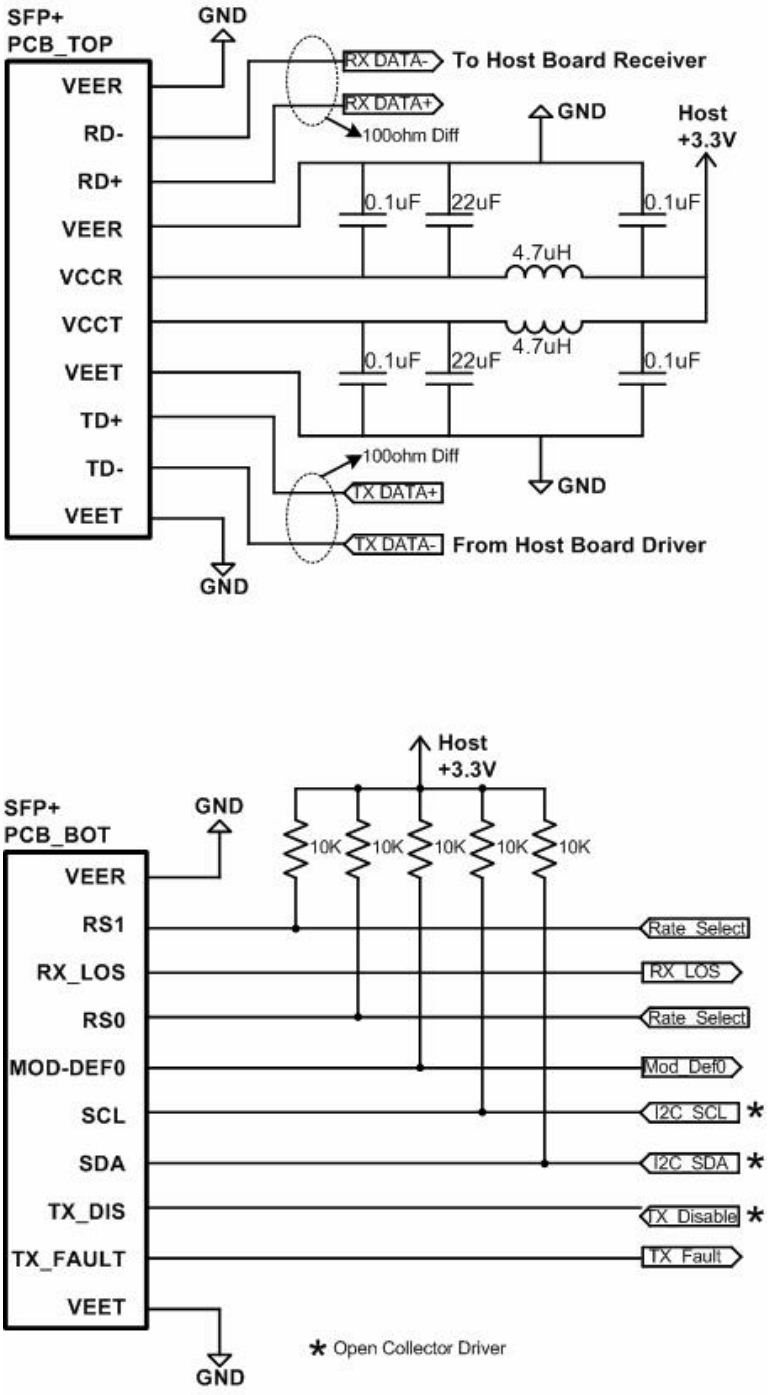

Figure4

Dimensions

Comply to SFF-8432 rev. 5.0, the improved Pluggable form factor specification.
(Not describe size tolerance reference: X.X±0.10 X.XX±0.05 X.XXX±0.01)

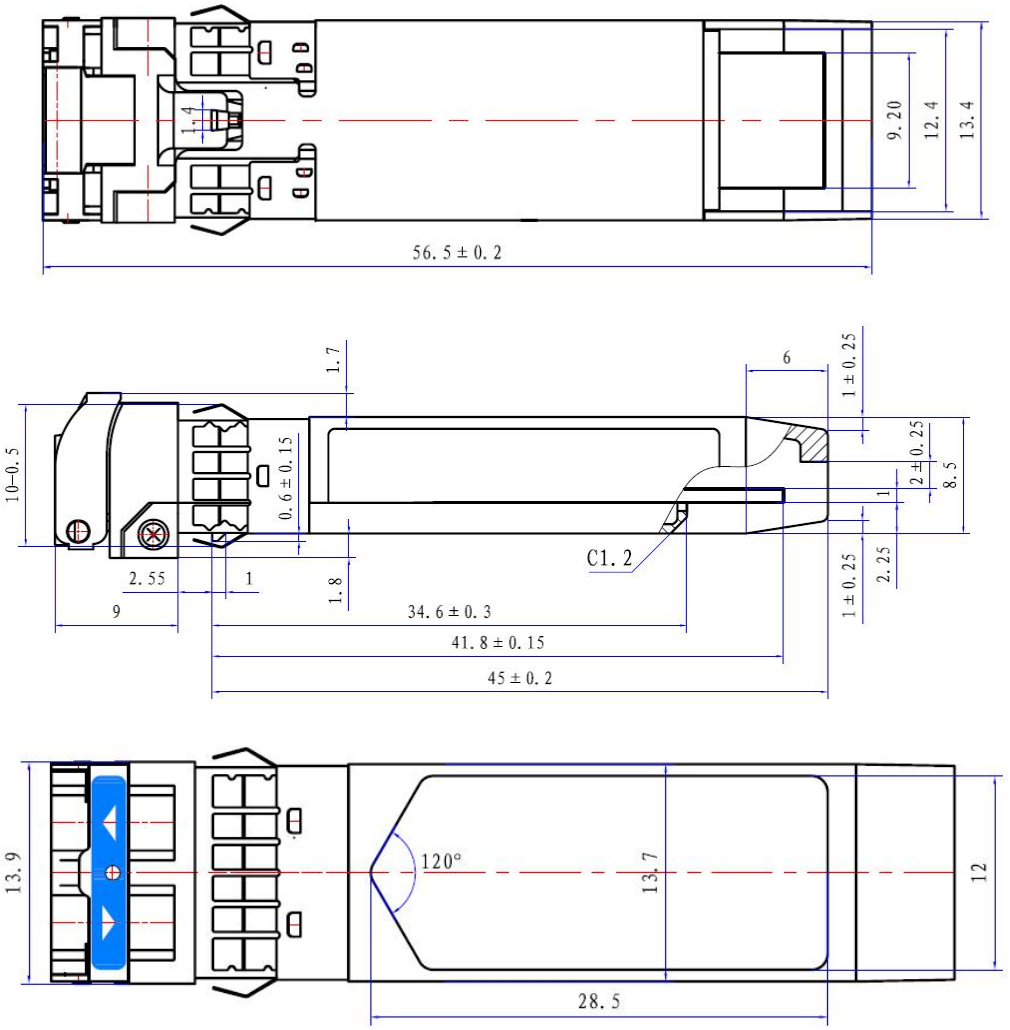

Figure5

Ordering Information

Part No.	Specification								
	Pack	Rate	Tx	Pout	Rx	S	Top	Reach	Others
MTRS-2E30-01	SFP+	10G	1310nm DFB	-6~-1dBm	PIN-TIA	≤-14.4dBm	0～70℃	10km	DDM/RoHS

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